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09/992,076	11/13/2001	Craig Nemecek	CYPR-CD01210M	4880

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EXAMINER

PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/992,076

Applicant(s)

NEMECEK, CRAIG

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: ____.

DETAILED ACTION

Claims 1-20 have been presented for examination. Claims 1-20 have been rejected.

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Figs. 2 and 3 are partially hand drawn. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: page 15, lines 22-25 makes reference to "a production five wires Category Five patch cable" which is unknown in the art. A category five cable, as known in the art and defined by published standards, has four twisted pairs of wires. When addressing this, no new matter should be added.

Appropriate correction is required.

Technology Background

To facilitate discussion of the prior art, the Examiner provides the following technology background.

The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000) provides the following definitions:

- **execution trace** A record of the sequence of instructions executed during the execution of a computer program. Often takes the form of a list of code labels encountered as the program executes. *Synonym:* code trace. See *also:* subroutine trace; variable trace; retrospective trace; symbolic trace.
- **trace (2) (A)** A record of the execution of a computer program, showing the sequence of instructions executed, the names and values of variables, or both. Types include execution trace, retrospective trace, subroutine trace, symbolic trace, variable trace. **(B)** To produce a record as in definition (A). **(C)** To establish a relationship between two or more products of the development process; for example, to establish a relationship between a given requirement and the design element that implements that requirement. **(3)** To execute the component steps of a computer program, displaying the state of selected system resources after each step. **(4)** A diagnostic fault isolation program that uses a probe on a tester.
- **breakpoint (1) (A) (computer routine)** Pertaining to a type of instruction, instruction digit, or other condition used to interrupt or stop a computer at a particular place in a routine when manually requested. **(B) (computer routine)** A place in a routine where such an interruption occurs or can be

made to occur. **(2) (software)** A point in a computer program at which execution can be suspended to permit manual or automated monitoring of program performance or results. Types include code breakpoint, data breakpoint, dynamic breakpoint, epilog breakpoint, programmable breakpoint, prolog breakpoint, static breakpoint. *Note:* A breakpoint is said to be set when both a point in the program and an event that will cause suspension of execution at that point are defined; it is said to be initiated when program execution is suspended. **(3)** A position within a pattern set where the pattern may be segmented into multiple independent bursts while still achieving predictable behavior of the device.

- **breakpoint instruction (A)** A computer instruction that causes program flow to be halted. *See also:* address stop. **(B)** A computer instruction that causes program flow to be redirected to a monitor or debugging system. *Synonym:* breakpoint halt; dynamic stop.
- **address stop** An address that, when it is encountered by a program, causes the program to halt execution. *See also:* breakpoint instruction; instruction address stop.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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3. Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites the phrase "a computer system capable of comparing a content of the first memory against a content of the second memory to verify said lock step". The meaning of a computer system *capable* of performing a task is vague and indefinite as it is unknown whether a system of the prior art must perform that task in order to teach the claimed invention. The Examiner presumes that the computer system *does* perform the task of comparing in the claimed invention.

4. Claims 2 and 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 2 and 16 recite the acronym "POD" without first defining the term. The standard language defining its use should accompany the first appearance of the acronym in the claims. The Examiner presumes the intended definition is "external circuit board".

5. The term "substantially" in claims 3 and 17 is a relative term which renders these claims indefinite. The term "substantially" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. When assessing the prior art, it is impossible to determine the extent to which a microcontroller must be copied into an FPGA in order to teach the claimed limitation. The Examiner interprets these claims omitting the word "substantially".

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6. Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 4 recites the acronym "SRAM" without first defining the term. The standard language defining its use should accompany the first appearance of the acronym in the claims. The Examiner presumes the intended definition is "static random access memory".

7. Claims 5 and 18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear exactly what is meant by "register files" or why "register files" should be regarded as patentably distinct from any other type of computer file. The Examiner respectfully requests clarification including citations of support in the specification for "register files".

8. Claim 8 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unknown what is meant by "a content of the first CPU" and "a content of the second CPU". To the best of the Examiner's understanding, a person of ordinary skill in the art of software debugging would not recognize a CPU as having contents. The Examiner respectfully requests clarification including citations of support in the specification for "a content of a CPU".

9. Claim 10 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

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applicant regards as the invention. There are several grounds for rejection of claim 10 under 35 U.S.C. § 112. Claim 10 recites a step that appears to be human cognition. Claim 10 recites a step that produces no result, therefore it is unclear how the step relates to the invention as a whole or what is necessary in the prior art to teach the step. Claim 10 recites "locating an error", however the definition of "an error" is omitted. It is unclear if "an error" refers to a hardware exception (such as dividing by zero, an error recognized by a processor) or a software bug (where semantically perfect code performs properly, however the code was not written as intended) or both.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-2, 4-11, 13-16, and 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,911,059 to Profit, Jr. (Profit).

Regarding claim 1, Profit teaches:

a microcontroller installed on a test circuit, wherein the microcontroller includes a first memory and a first CPU (Fig. 7, references 202, 204, and 206);
an ICE including a second memory and a second CPU coupled to a computer system (Fig. 7, references 214, 210, 212; column 6, lines 25-48);

the ICE emulates the microcontroller (column 6, lines 29-43);
the microcontroller and the ICE run the code in lockstep (column 6, lines 25-48;
column 11, lines 40-43);
an interface for coupling the test circuit and the ICE enabling data transmission
between the test circuit and the computer system (Fig. 7, reference 220;
column 7, line 49 – column 8, line 2);
the computer system capable of comparing a content of the first memory against
a content of the second memory to verify said lock step (column 12, lines
24-35; column 14, lines 44-58; direct comparison of a *clock count* stored
memory content).

Official notice is taken that the term *microcontroller* refers to a single unit usually comprising central processing unit, memory, and I/O ports. As Profit teaches an emulator unit that contains at least these features (Fig. 7, reference 202), it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that Profit's emulator is readily adaptable to accept microcontrollers, as would be desired by a person whose goal it is to develop and debug code for microcontrollers.

Regarding claim 2, Profit teaches installing the microcontroller on an external circuit board (column 7, lines 15-30).

Regarding claim 4, Profit does not explicitly teach using SRAM. Official notice is taken that SRAM is extremely well known. It would have been obvious to a person of

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ordinary skill in the art at the time of Applicants' invention to use extremely well known technologies when implementing the system taught by Profit.

Regarding claim 5, the Examiner cannot grant patentable weight to the irrelevant contents of the memory. That said, Profit teaches memory, and it would have been obvious to a person of ordinary skill in the art to store files in the memory. The Examiner can find no connection between the limitations of claim 5 and the invention as a whole.

Regarding claim 6, official notice is taken that modern CPUs have a program counter. Further, Profit teaches that the first and second CPUs have a clock count, functionally equivalent to program counters, which are synchronized to maintain the CPUs in lock-step (column 12, lines 24-35).

Regarding claims 7 and 8, this claim recites a limitation that amounts to human cognition. The Examiner cannot grant patentable weight to the mental processes a user of the system may or may not undertake. That said, Profit teaches a system for developing or debugging code. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use Profit's system as it was designed, that is to say, to compare contents of the memory during debugging operations.

Additionally, please see MPEP 2114, "Manner of operating the device does not differentiate apparatus claim from the prior art".

2. Regarding claim 9, Profit teaches a method for debugging microcontroller code comprising:

initializing memory of an ICE and a second memory of a microcontroller with microcontroller test code (Fig. 7, references 206, 22; column 6, lines 29-35);

executing the microcontroller test code on the microcontroller and on the ICE in lock step (column 6, lines 38-48; column 11, lines 40-43);

verifying lock step execution by comparing content of the first memory and content of the second memory (column 12, lines 25-35, comparing the "clock count");

and if lock step is verified, continuing execution of the microcontroller test code (column 12, lines 25-35).

Profit does not explicitly teach "if lock step execution is not verified, reporting an error and saving an execution history using a trace buffer coupled to the ICE". However official notice is taken that reporting an error when an exception occurs is generally referred to as "error or exception handling" and is well known in the art. Official notice is taken that the use of an execution history trace buffer is a standard debugging tool and well known in the art. Profit explicitly teaches the inclusion of standard software debugging tools (column 6, lines 49-60) which a person of ordinary skill in the art at the time of Applicants' invention would recognize as including an execution history trace buffer. Therefore it would have been obvious to a person of ordinary skill in the art at

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the time of Applicants' invention, in combination with his own knowledge of the particular art and at Profit's explicit suggestion, to incorporate error or exception handling and standard debugging tools such as an execution history trace buffer. This combination could be readily implemented using techniques well known in the art.

Regarding claim 10, the claim recites the well-known process of human cognition known as using an execution trace to debug a program. That said, Profit teaches a system for developing or debugging code. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use Profit's system as it was designed or as represented by the combination formed in the rejection of claim 9 to debug code. Please see MPEP 2114.

Regarding claim 11, Profit teaches verifying lock step by comparing a clock count (column 12, lines 25-35). A person of ordinary skill in the art would recognize a clock count, an instruction pointer, or other equivalent means by which a processor marks its progress through a body of instruction code as a register value.

Regarding claim 13, Profit teaches that the microcontroller is a production microcontroller (column 6, lines 5-24).

Regarding claim 14, Profit does not explicitly teach the use of breakpoints, however Profit does teach halting the execution of the microcontroller test code (column

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9, lines 40-61) and verifying lock step execution by comparing content of the first memory and content of the second memory while the execution is halted (column 12, lines 25-35). Profit does explicitly teach using standard debugging techniques as known in the art (column 6, lines 49-60). Official notice is taken that breakpoints are a fundamental and extremely well known technique for debugging software. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art and at Profit's explicit suggestion, to use breakpoints when debugging the code.

3. The system of claim 15 recites the limitations of claim 1 with the additional limitation of "a computer system coupled to the ICE for controlling a debugging operation on the microcontroller code". As Profit clearly teaches such a computer system (Fig. 7, reference 214; column 6, lines 49-60), claim 15 is rejected for this reason and those given above for claim 1.

Regarding claim 16, Profit teaches installing the microcontroller on an external circuit board (column 7, lines 15-30).

Regarding claim 18, the Examiner cannot grant patentable weight to the irrelevant contents of the memory. That said, Profit teaches memory, and it would have been obvious to a person of ordinary skill in the art to store files in the memory. The

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Examiner can find no connection between the limitations of claim 5 and the invention as a whole.

Regarding claim 19, this claim recites a limitation that amounts to human cognition. The Examiner cannot grant patentable weight to the mental processes a user of the system may or may not undertake. That said, Profit teaches a system for developing or debugging code. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use Profit's system as it was designed, that is to say, to compare contents of the memory during debugging operations. Please see MPEP 2114.

Regarding claim 13, Profit teaches that the microcontroller is a production microcontroller (column 6, lines 5-24).

4. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Profit as applied to claim 1 above, and further in view of US Patent No. 6,173,419 to Barnett.

Regarding claim 3, Profit does not explicitly teach that the microcontroller is copied in an FPGA of the ICE.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55). Barnett teaches that such a system is advantageous by allowing it to be reconfigured (column 5, lines 31-36).

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the FPGA emulator taught by Barnett with the software testing system of Profit in order to enjoy the well-known advantages of hardware emulation, such as speed, as well as the advantages of being reconfigurable, as explicitly taught by Barnett. The combination could be achieved by implementing the hardware simulator of Profit as an external emulator implemented in an FPGA.

5. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Profit as applied to claim 9 above, and further in view of Barnett.

Regarding claim 12, Profit does not explicitly teach that the microcontroller is implemented in an FPGA of the ICE.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55). Barnett teaches that such a system is advantageous by allowing it to be reconfigured (column 5, lines 31-36).

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the FPGA emulator taught by Barnett with the software testing system of Profit in order to enjoy the well-known advantages of hardware emulation, such as speed, as well as the advantages of being reconfigurable, as explicitly taught by Barnett. The combination could be achieved by implementing the hardware simulator of Profit as an external emulator implemented in an FPGA.

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6. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Profit as applied to claim 15 above, and further in view of Barnett.

Regarding claim 17, Profit does not explicitly teach that the microcontroller is copied in an FPGA of the ICE.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55). Barnett teaches that such a system is advantageous by allowing it to be reconfigured (column 5, lines 31-36).

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the FPGA emulator taught by Barnett with the software testing system of Profit in order to enjoy the well-known advantages of hardware emulation, such as speed, as well as the advantages of being reconfigurable, as explicitly taught by Barnett. The combination could be achieved by implementing the hardware simulator of Profit as an external emulator implemented in an FPGA.

Conclusion


Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

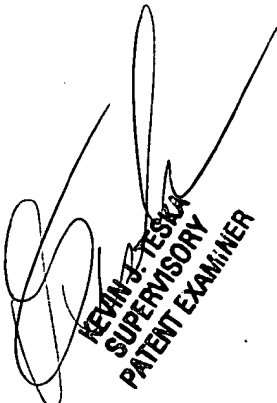
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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